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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,412	NABESAKO ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *application filed on 23 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 19-32 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to **a single paragraph** on a separate sheet within the range of **50 to 150 words**.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: **Demultiplexer for handling different type of multiplexing format**.

Claim Objections

4. Claim 8 is objected to because of the following informalities: Appropriate correction is required.

Claim 8 recites, "...the controller generates from the micro-code read out from the command memory **a control signal** for actuating..." in lines 1-2. For clarity it is suggested to insert commas "," as in "...the controller generates, from the micro-code read out from the command memory, a control signal for actuating..." in line 1-2.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "**the** headers" in line 8. There is insufficient antecedent basis for this limitation in the claim. Claim 1 recites, "each **component**" in page 37, line 3. It is unclear whether "component" refers to a data input, a first storage, a second storage, a calculating unit, an output destination determining unit, a separator, a command memory, and/or a counter.

Claim 4 recites, the limitation "**the** length" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites, the limitation "**the** continuity" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites, the limitation "**the** head" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 7 recites, "**it**" in line 4. It is unclear whether "it" means: the input digital data, the header of each packet, or a bit manipulating process.

Claim 8 recites, the limitation "**the** shifting action" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites, the limitation "**the** byte endian" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-3,5,9-12, and 14 are also rejected since they are depended on rejected claim 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler (U.S. 5,602,920) in view of Kanzaki (U.S. 5,983,018).

Regarding Claim 1, Bestler discloses a demultiplexer (see FIG. 2, DCAM Xport Demux 20) for separating desired packets (see FIG. 1, packets for Audio decomp 26 and video decomp 24; see col. 3, lines 29-32) for output from an input digital data (see FIG. 1, a packet data stream from IF Amp Demod 18; see col. 2, lines 49-54) which has different format packets multiplexed in a given manner (see col. 2, lines 49-54; multiplexed MPEG data which consist of audio and video packets; see col. 3, lines 4-10), comprising:

a data input (see FIG. 3, Input side of Xport stream interface 48) for receiving the input digital data (see col. 4, lines 29-33);

a first storage (a shift register) (see FIG. 3, Xport stream interface 48) for storing and transferring the input digital data received at the data input (see col. 4, lines 30-35; note that X-port stream interface stores and transfers data to Xport Header parser 49);

a second storage (a group of registers) (see FIG. 3, a combined system of Xport Header parser 49 and PID comparator and processor 52) for extracting and storing the headers of the packets (see col. 4, lines 35-45 and see col. 7, lines 25-30; transport header which comprises Packet Identifier, PID, is parsed/extracted and stored in the registers) from the input digital data stored in the first storage (a shift register) (see col. 4, lines 32-60);

a calculating unit (see FIG. 3, PID comparator and processor 52) for analyzing the headers of the packets stored in the second storage (a group of registers) (see col. 4, lines 35-59; note that PID comparator and processor 52 analyzes the header and PID by comparing);

an output destination determining unit (see FIG. 3, a combined system of PID comparator and processor 52 and routing manager 68) for determining the destination of the packets (see col. 4, lines 55-60; see col. 5, lines 6-12; destination is determined if PID match) from a packet identifier (see col. 4, lines 35-45; Packet identifier, PID) which is contained in the headers of the packets stored in the second storage (a group of registers) (see col. 4, lines 35-45 and see col. 7, lines 25-30; transport header which comprises Packet Identifier, PID);

a separator (see FIG. 3, a combined system of data buffer 70 and DRAM control and interface 72) arranged responsive to a result of the calculating action of the calculating unit (see col. 4, lines 50-57; an identified packet and its payload is the result) and an output of the

output destination determining unit (see col. 5, lines 9-14; a matched PID for either video or audio packet is the output) for separating the desired packets from the input digital data received from the first storage (a shift register) (see col. 5, lines 10-16; note that DRAM control and interface 72 divides/separates/demultiplexes the received multiplexed data from Xportstream interface 48, via data buffer 70 and payload crypto device 50, into the output channel #1 or # 2);

a command memory (see FIG. 3, DCAM circuits 72 and programmable memory OPTM 72a) for storing micro-codes (see FIG. 3, instructions or codes) provided for selecting a controlling action in each multiplexing format (see FIG. 3, CPU 54; see col. 4, lines 60 to col. 5, lines 6; note that DCAM 72 stores codes/instructions such as authorization, serial number and decryption keys for each multiplexed packet format.);

a controller (see FIG. 3, CPU 54) for controlling the action of each component with the micro-code read out from the command memory (see col. 4, lines 55 to col. 5, lines 16; see col. 7, lines 16-50; CPU 54 controls each component (i.e. 49,52,48,68,50,70,72) to processes the multiplexed data according to stored codes from DCAM 72 and OPTM 72a); and

a system clock controller (see FIG. 3, a combined system of payload sync DPLL 47) for extracting the timing data from the input digital data stored in the first storage (a shift register; see col. 4, lines 29-31; see col. 9, lines 14-45; DPLL extract timing from input data) and controlling a system clock (see FIG. 3, sync circuits 106 comprises system clock) with the timing data (see col. 7, lines 52-67, see col. 8, lines 60 to col. 9, lines 45; note that DPLL is used to synchronize the system clock.)

Bestler does not explicitly disclose a counter for determining an execution address of the micro-code stored in the command memory, and controller executing address determined by the counter. However, these limitations are well known in the art of computer. Any personal computer have a program/command memory which stores the instructions/commands/codes, a counter or clock which determine the execution address/number of each instruction, and CPU which process the code/instruction from the program memory in accordance the clock/counter. In particular, Kanzaki teaches a command memory (see FIG. 3, Program Memory 15) for storing micro-codes (see col. 1, lines 44-46; 56-57; stores user programs) provided for selecting a controlling action (see col. 1, lines 44-57; programs for debugging actions), a counter (see FIG. 6, program counter 40) for determining an execution address (see col. 6, lines 34-37) of the micro-code stored in the command memory (see col. 6, lines 32-41), and a controller (see FIG. 3, CPU 10) for controlling the action of each component (see FIG. 3, RAM 14, program memory 15, debug support circuit 17, flag circuit 30) with the micro-code read out from the command memory by the execution address determined by the counter (see col. 4, lines 25-35; see col. 6, lines 30-45; note that CPU process each component with the program/instruction from the program memory determined by the program counter). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a program counter and its interaction with CPU and program memory, as taught by Kanzaki in the system of Bestler, so that it would allow the program counter to decremented without the intervention of software, thereby, making the process faster and also would reduce the cost of adding extra hardware; see Kanzaki col. 3, line 22-34, 49-56.

Regarding Claim 8, Bestler discloses the controller generates from the micro-code read out from the command memory a control signal for actuating one or more components at one time (see col. 4, lines 25-44; see col. 6, lines 1-19; see FIG. 1, CPU 54 connects to components within the system 20 in order to demultiplex the multiplexed data stream. It is well known in the art that CPU sends a control signal at least one time in order to instruct/command the component(s)). Kanzaki teaches the controller generates from the micro-code read out from the command memory a control signal (see FIG. 3, a control signal line) for actuating one or more components at one time (see col. 4, lines 29-51).

Regarding Claim 14, Kanzaki discloses a data writing means (see FIG. 1, microcomputer 1) for writing the micro-codes in the command memory (see col. 1, lines 44-45; the microcomputer contains a data writing means in order to write the user program into the program memory).

9. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Goody (U.S. 6,097,721).

Regarding Claim 2, neither Bestler nor Kanzaki explicitly disclose a contents addressable memory. However, using CAM is well known in the art. In particular, Goody discloses a contents addressable memory (see FIG. 7, CAM, contents addressable memory, 710; abstract; see col. 7, lines 54-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide CAM, as taught by Goody, in the combined system of Bestler and Kanzaki, so that it would identify signals for a set of communication device; see Goody col. 2, line 14-25.

Regarding Claims 3, Bestler in view of Kanzaki discloses all of the limitations as recited in claim 1 above. Neither Bestler nor Kanzaki explicitly disclose a data writing means for writing in a built-in memory. However, a data writing means for writing data for writing in a built-in memory of CAM is well known in the art. In particular, Goody discloses a data writing means (see FIG. 8, control circuitry 805 control the writing/reading) for writing data (see FIG. 8, Cell type and counter values) for determining the destination (see col. 9, lines 60-67; the received cell is destined as telephony cell or non-telephony cell) in a built-in memory (see FIG. 8, comparators and memory 810) of the output destination determining unit (see FIG. 8, CAM 710); see col. 8, lines 40 to col. 10, lines 21). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide CAM with memory and comparator to identify the type of cell in order determined the cell destination, as taught by Goody, in the combined system of Bestler and Kanzaki, so that it would identify signals for a set of communication device; see Goody col. 2, line 14-25.

10. Claims 4 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Anderson (U.S. 5,761,453).

Regarding Claims 4, Bestler in view of Kanzaki discloses all of the limitations as recited in claim 1 above. Neither Bestler nor Kanzaki explicitly disclose a register acting as a counter for managing the length of each packet. However, a register acting as a counter for managing the length of each packet is well known in the art. In particular, Anderson discloses a register acting as a counter (see FIG. 2, DMA_Counter register 24) for managing the length of each packet in the input digital data (see FIG. 4A, steps 30,32,34; see col. 4, lines 9-31; the DMA_count register managing/counting/determining the length of the packet

in the input data). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide DMA_counter register which counts the length of the input packet, as taught by Anderson, in the combined system of Bestler and Kanzaki, so that it would increase the througput of serial data in a computer system when a data packet is of unknown length; see Anderson col. 2, line 5-44.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Bartkoviak (U.S. 5,282,153).

Regarding Claims 5, Neither Bestler nor Kanzaki explicitly disclose an arithmetic logic unit. However, utilizing arithmetic logic unit is well known in the art. In particular, Bartkoviak discloses an arithmetic logic unit (see FIG. 1, Arithmetic Logic Unit 12; see col. 3, lines 9-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide arithmetic logic unit, as taught by Bartkoviak, in the combined system of Bestler and Kanzaki, so that it would perform a number of different digital arithmetic operation in an efficient manner thus reduce the number of operation cycles; see Bartkoviak col. 1, line 52 to col. 2, lines 56.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Nakamura (U.S. 6,393,082).

Regarding Claims 6, Neither Bestler nor Kanzaki explicitly disclose a dedicated circuit for detecting the continuity between packets. However, utilizing a dedicated circuit for detecting the continuity between packets in the input digital data is well known in the art. In particular, Nakamura discloses a dedicated circuit (see FIG. 2, Signal Synchronism detecting

circuit) for detecting the continuity (see col. 5, lines 55-67; continuity bits) between packets in the input digital data (see abstract; see col. 6, lines 15-20, 52-60; note that the detecting circuit detects the continuity bits between data group in the received data signal). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide signal synchronism detecting circuit to detect the continuity bits, as taught by Nakamura, in the combined system of Bestler and Kanzaki, so that it provide relatively small circuit scale and capable of surely performing the conversion with a minimized data transfer delay and with a reduce power consumption and by detecting the continuity bits, the system can determine when the delimiter of the data group; see Nakamura col. 3, line 25-45.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Harriman (U.S. 5,898,687).

Regarding Claims 7, Neither Bestler nor Kanzaki explicitly disclose a dedicated circuit for subjecting the head of each packet in the input digital data to a bit manipulating process and storing it in the second storage. However, manipulating an extracted/parsed header of the incoming signal and storing it in the storage is well known in the art. In particular, Harriman discloses a dedicated circuit (see FIG. 1, ITF 120, Input Translator function) for subjecting the head of each packet (see FIG. 1, receiving extracted header from extract 114) in the input digital data (see FIG. 1, input cell from input ports 102) to a bit manipulating process (see col. 4, lines 40-50; ITF process the address, key, priority in the header) and storing it in the second storage (see FIG. 1, Unicast queues 130 or multicast

engine 200; see col. 4, lines 46-52,65-67; the processed header information is forward and stored in 130 or 200). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a circuit that manipulate the header of each cell and store them in the queue/memory, as taught by Harriman, in the combined system of Bestler and Kanzaki, so that it would increase the switching rate with minimal buffer capacity by processing headers separately; see Harriman col. 1, line 60-65, see col. 2, lines 19-30.

14. Claims 9 and 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Kalkunte (U.S. 6,115,356).

Regarding Claim 9, Neither Bestler nor Kanzaki explicitly disclose wherein the data input includes an input buffer for temporarily saving the input digital data. However, wherein the data input includes an input buffer for temporarily saving the input digital data is well known in the art. In particular, Kalkunte discloses an input buffer (see FIG. 1, Input buffer 18) for temporarily saving the input digital data (see col. 3, lines 40-50, see col. 4, lines 35-46). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide input buffer to store packets, as taught by Kalkunte, in the combined system of Bestler and Kanzaki, so that it would store or hold the packets before sending them to the output buffer when there is a congestion and to minimize the head of line blocking; see Kalkunte col. 1, line 4-15, 60-67; see col. 3, lines 45-50.

Regarding Claim 10, Neither Bestler nor Kanzaki explicitly disclose wherein the input buffer when receiving the input data has a data read out in synchronism with the shifting action of the first storage. However, Kalkunte discloses wherein the input buffer (see

FIG. 1, Input Buffer 18) when receiving the input digital data (see FIG. 1, receiving packet from 16) has a data read out in synchronism (see FIG. 1, Data Monitor 30 and Congestion Monitor 24) with the shifting action of the first storage (see FIG. 1, output buffer 18; see col. 4, lines 49-61; see col. 6, lines 10-31; both data monitor and congesting monitor to ensures the packets store in input buffer is synchronized with packets in output buffer.) Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide synchronizing mechanism between input and output buffers, as taught by Kalkunte, in the combined system of Bestler and Kanzaki, so that it would minimize congestion and the head of line blocking; see Kalkunte col. 1, line 4-15, 60-67; see col. 3, lines 45-50.

15. Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of Kovacevic (U.S. 6,778,533).

Regarding Claim 11, Bestler in view of Kanzaki discloses all of the limitations as recited in claim 1 above. Neither Bestler nor Kanzaki explicitly disclose a plurality of buffer memories for storing the packets. However, wherein the data input includes an input buffer for temporarily saving the input digital data is well known in the art. In particular, Kalkunte discloses a plurality of buffer memories (see FIG. 5, Video memory 471 and System memory 472) for storing the packets separated by the separator (see FIG. 5, Buffer controller 460; see col. 7, lines 40-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide buffer memories to store different type of data, as taught by Kovacevic, in the combined system of Bestler and Kanzaki, so that the

system does not need to access memory space which eliminates delays, and it would also allow more flexibility and improved performance; see Kovacevic col. 4, line 51-56; see col. 7, lines 46-52.

16. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bestler in view of Kanzaki, as applied to claim 1 above, and further in view of well established teaching in art.

Regarding Claim 12, Bestler in view of Kanzaki discloses all of the limitations as recited in claim 1 above. Neither Bestler nor Kanzaki explicitly disclose a single buffer memory, which has an array of storage regions for storing the packets. However, Official Notice is taken that both the concept and the advantages of providing a single buffer memory, which has an array of storage regions for storing the different packets, is well known and expected in the art. It is well known in the art that a single memory has array/series of storage/spaces/regions to store different packets. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a single memory with array/series of storage/space/regions to store packets, as taught by well established teaching in art, in the combined system of Bestler and Kanzaki, so that it would enable storing of different packets in a signal memory.

Regarding Claim 13, Bestler in view of Kanzaki discloses all of the limitations as recited in claim 1 above. Neither Bestler nor Kanzaki explicitly disclose means for modifying the byte endian. However, Official Notice is taken that both the concept and the advantages of providing means for modifying the byte endian, is well known and expected in the art. It is

well known in the art that a byte endian can be modified to meets it specific needs. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the byte endian, as taught by well established teaching in art, in the combined system of Bestler and Kanzaki, so that it would meet the demultiplexer/separator would meet its specific needs of separation/demultiplexing.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
11/19/04

BRIAN NGUYEN
PRIMARY EXAMINER